What is claimed is:

1. A method of forming a dielectric layer comprising:

forming a layer of hafnium oxide by atomic layer deposition; and

forming a layer of a lanthanide oxide by electron beam evaporation, wherein the layer of hafnium oxide is in contact with the layer of lanthanide oxide.

2. The method of claim 1, wherein the method further includes forming the layer of hafnium oxide on a substrate and forming the layer of lanthanide oxide on the layer of hafnium oxide.

3. The method of claim 1, wherein the method further includes forming the layer of lanthanide oxide on a substrate and forming the layer of hafnium oxide on the layer of lanthanide oxide.

4. The method of claim 1, wherein the method further includes controlling the forming of the layer of hafnium oxide and the forming of the layer of the lanthanide oxide to form a lanthanide oxide/hafnium oxide nanolaminate.

5. The method of claim 1, wherein the method further includes limiting a combined thickness of lanthanide oxide layers to between about 2 nanometers and about 10 nanometers.

6. The method of claim 1, wherein the method further includes limiting a combined thickness of hafnium oxide layers to a thickness between about 2 nanometers and about 10 nanometers.

7. The method of claim 1, wherein the method further includes forming multiple layers of lanthanide oxide, each layer of lanthanide oxide limited to a thickness between about 2 nanometers and about 10 nanometers.

8. The method of claim 1, wherein forming a layer of a lanthanide oxide includes forming an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

9. The method of claim 1, wherein the method further includes maintaining the substrate at a temperature ranging from about 100 °C to about 150 °C.

10. The method of claim 1, wherein the method further includes adding oxygen during the electron beam evaporation of the layer of lanthanide oxide.

11. A method of forming a dielectric layer comprising:

forming a layer of hafnium oxide on a substrate by atomic layer deposition using a HfI_4 precursor; and

forming a layer of a lanthanide oxide on the layer of hafnium oxide by electron beam evaporation.

12. The method of claim 11, wherein the method further includes controlling the forming of the layer of hafnium oxide and the forming of the layer of the lanthanide oxide to form a lanthanide oxide/hafnium oxide nanolaminate.

13. The method of claim 11, wherein the method further includes limiting a combined thickness of lanthanide oxide layers to a thickness between about 2 nanometers and about 10 nanometers.

14. The method of claim 11, wherein forming a layer of a lanthanide oxide includes forming an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

15. The method of claim 11, wherein the method further includes maintaining the substrate at a temperature ranging from about 100 °C to about 150 °C.

16. A method of forming a capacitor, comprising:

forming a first conductive layer on a substrate;

forming a dielectric layer on the first conductive layer; and

forming a second conductive layer on the dielectric layer, wherein forming the dielectric layer includes:

forming a layer of hafnium oxide on the first conductive layer by atomic layer deposition using a HfI_4 precursor; and

forming a layer of a lanthanide oxide on the layer of hafnium oxide by electron beam evaporation, wherein the layer of lanthanide oxide is limited to between about 2 nanometers and about 10 nanometers.

17. The method of claim 16, wherein the method further includes controlling the forming of the layer of hafnium oxide and the forming of the layer of the lanthanide oxide on the layer of hafnium to form a lanthanide oxide/hafnium oxide nanolaminate.

18. The method of claim 16, wherein forming a layer of a lanthanide oxide includes forming an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

19. The method of claim 16, wherein the method further includes maintaining the substrate at a temperature ranging from about 100 °C to about 150 °C.

20. A method of forming a transistor comprising:

forming a source region and a drain region in a substrate, the source region and the drain region separated by a body region;

forming a dielectric layer on the body region between the source and drain regions, the dielectric layer containing a nanolaminate of hafnium oxide and a lanthanide oxide; and

coupling a gate to the dielectric layer, wherein forming the nanolaminate includes:

forming a layer of hafnium oxide by atomic layer deposition; and

forming a layer of a lanthanide oxide by electron beam evaporation.

21. The method of claim 20, wherein the method further includes limiting a combined thickness of lanthanide oxide layers to a thickness between about 2 nanometers and about 10 nanometers.

22. The method of claim 20, wherein the method further includes forming multiple layers of lanthanide oxide, each layer limited to a thickness of lanthanide oxide layers to between about 2 nanometers and about 10 nanometers.

23. The method of claim 20, wherein forming a layer of a lanthanide oxide includes forming an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

24. The method of claim 20, wherein forming a layer of a hafnium oxide by atomic layer deposition includes using a hafnium halide as a precursor.

25. The method of claim 20, wherein the method further includes maintaining the substrate at a temperature ranging from about 100 °C to about 150 °C.

26. The method of claim 20, wherein the method further includes adding oxygen during the electron beam evaporation of the layer of lanthanide oxide.

27. A method of forming a memory comprising:

forming a number of access transistors including forming a dielectric layer on a body region in a substrate between a source region and a drain region; and

forming a number of word lines, each word line coupled to one of the number of access transistors, wherein forming the dielectric layer includes:

forming a layer of hafnium oxide on the body region by atomic layer deposition; and

forming a layer of a lanthanide oxide on the layer of hafnium oxide by electron beam evaporation.

28. The method of claim 27, wherein the method further includes limiting a combined thickness of lanthanide oxide layers to between about 2 nanometers and about 10 nanometers and limiting a combined thickness of hafnium oxide layers to between about 2 nanometers and about 10 nanometers.

29. The method of claim 27, wherein the method further includes forming multiple layers of lanthanide oxide, each layer limited to a thickness of lanthanide oxide layers to between about 2 nanometers and about 10 nanometers.

30. The method of claim 27, wherein forming a layer of a lanthanide oxide includes forming an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

31. The method of claim 27, wherein forming a layer of a hafnium oxide by atomic layer deposition includes using a hafnium halide as a precursor.

32. The method of claim 27, wherein the method further includes maintaining the substrate at a temperature ranging from about 100 °C to about 150 °C.

33. The method of claim 27, wherein the method further includes adding oxygen during the electron beam evaporation of the layer of lanthanide oxide.

34. A method of forming an electronic system comprising:

providing a controller; and

coupling a device to the controller, wherein at least one of the controller and the device includes a dielectric layer having a nanolaminate of hafnium oxide and a lanthanide oxide, wherein forming the nanolaminate includes:

forming a layer of hafnium oxide by atomic layer deposition; and

forming a layer of a lanthanide oxide by electron beam evaporation.

35. The method of claim 34, wherein the method further includes limiting a combined thickness of lanthanide oxide layers to between about 2 nanometers and about 10 nanometers.

36. The method of claim 34, wherein the method further includes limiting a combined thickness of hafnium oxide layers to between about 2 nanometers and about 10 nanometers.

37. The method of claim 34, wherein the method further includes forming multiple layers of lanthanide oxide, each layer limited to a thickness of lanthanide oxide layers to between about 2 nanometers and about 10 nanometers.

38. The method of claim 34, wherein forming a layer of a lanthanide oxide includes forming an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

39. The method of claim 34, wherein forming a layer of a hafnium oxide by atomic layer deposition includes using a hafnium halide as a precursor.

40. The method of claim 34, wherein the method further includes maintaining the substrate at a temperature ranging from about 100 °C to about 150 °C.

41. The method of claim 34, wherein the method further includes adding oxygen during the electron beam evaporation of the layer of lanthanide oxide.

42. A device having a dielectric layer comprising:

an atomic layer deposited hafnium oxide layer; and

an electron beam evaporated lanthanide oxide layer, wherein the atomic layer deposited hafnium oxide layer is deposed adjacent to and contacting the electron beam evaporated lanthanide oxide layer.

43. The device of claim 42, wherein the atomic layer deposited hafnium oxide layer and the electron beam evaporated lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate.

44. The device of claim 42, further including electron beam evaporated lanthanide oxide layers, wherein the combined thickness of the electron beam evaporated lanthanide oxide layers is between about 2 nanometers and about 10 nanometers.

45. The device of claim 42, further including atomic layer deposited hafnium oxide layers, wherein the combined thickness of the atomic layer deposited hafnium oxide layers is between about 2 nanometers and about 10 nanometers.

46. The device of claim 42, wherein the atomic layer deposited hafnium oxide layer and the electron beam evaporated lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate having multiple layers of electron beam evaporated lanthanide oxide, each layer of electron beam evaporated lanthanide oxide limited to a thickness of between about 2 nanometers and about 10 nanometers.

47. The device of claim 42, wherein the electron beam evaporated lanthanide oxide layer includes an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

48. A capacitor, comprising:

a first conductive layer;

a dielectric layer containing a hafnium oxide/ lanthanide oxide nanolaminate disposed on the first conductive layer, the nanolaminate having one or more lanthanide oxide layers; and

a second conductive layer disposed on the dielectric layer, wherein the

hafnium oxide/ lanthanide oxide nanolaminate includes an electronic beam evaporated lanthanide oxide layer disposed on an atomic layer deposited hafnium oxide layer, the lanthanide layers of the nanolaminate having a combined thickness ranging from about 2 nanometers to about 10 nanometers.

49. The capacitor of claim 48, wherein the atomic layer deposited hafnium oxide layer is disposed on the first conductive layer.

50. The capacitor of claim 48, wherein hafnium oxide/ lanthanide oxide nanolaminate includes an electron beam evaporated lanthanide oxide layer disposed on the first conductive layer.

51. The capacitor of claim 48, wherein the electron beam evaporated lanthanide oxide layer includes an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

52. A transistor comprising:

a body region in a substrate between a source region and a drain region;

a dielectric layer disposed on the body region; and

a gate coupled to the dielectric layer, wherein the dielectric layer includes:

an atomic layer deposited hafnium oxide layer; and

an electron beam evaporated lanthanide oxide layer, wherein the atomic layer deposited hafnium oxide layer is deposed adjacent to and contacting the electron beam evaporated lanthanide oxide layer.

53. The transistor of claim 52, wherein the atomic layer deposited hafnium oxide layer and the electron beam evaporated lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate.

54. The transistor of claim 52, wherein the dielectric layer contains multiple electron beam evaporated lanthanide oxide layers with a combined thickness of the

multiple electron beam evaporated lanthanide oxide layers ranging from about 2 nanometers and about 10 nanometers.

55. The transistor of claim 52, wherein the dielectric layer contains multiple atomic layer deposited hafnium oxide layers with a combined thickness of the multiple atomic layer deposited hafnium oxide layers ranging from about 2 nanometers and about 10 nanometers.

56. The transistor of claim 52, wherein the atomic layer deposited hafnium oxide layer and the electron beam evaporated lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate having multiple layers of electron beam evaporated lanthanide oxide, each layer of electron beam evaporated lanthanide oxide limited to a thickness of between about 2 nanometers and about 10 nanometers.

57. The transistor of claim 52, wherein the electron beam evaporated lanthanide oxide layer includes an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

58. A memory comprising:

a number of access transistors, each access transistor including a gate coupled to a dielectric layer, the dielectric layer disposed on a body region in a substrate between a source region and a drain region; and

a number of bit lines, each bit line coupled to one of the number of access transistors, wherein the dielectric layer includes a hafnium oxide / lanthanide oxide nanolaminate having an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide with a combined thickness of electron beam lanthanide oxide layers in the nanolaminate having a thickness between about 2 nanometers and 10 nanometers.

59. The memory of claim 58, wherein the atomic layer deposited hafnium oxide layer is disposed on the first conductive layer.

60. The memory of claim 58, wherein hafnium oxide/ lanthanide oxide nanolaminate includes an electron beam evaporated lanthanide oxide layer disposed on the first conductive layer.

61. The memory of claim 58, wherein hafnium oxide/ lanthanide oxide nanolaminate includes a combined thickness of hafnium oxide layers ranging from about 2 nanometers to about 10 nanometers.

62. The memory of claim 58, wherein the electron beam evaporated lanthanide oxide layer includes an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.

63. An electronic system comprising:

a controller; and

an electronic device coupled to the controller, wherein at least one of the controller and the electronic device includes a dielectric layer, the dielectric layer including:

an atomic layer deposited hafnium oxide layer; and

an electron beam evaporated lanthanide oxide layer, wherein the atomic layer deposited hafnium oxide layer is deposed adjacent to and contacting the electron beam evaporated lanthanide oxide layer.

64. The electronic system of claim 63, wherein the atomic layer deposited hafnium oxide layer and the electron beam evaporated lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate.

65. The electronic system of claim 63, wherein the dielectric layer contains multiple electron beam evaporated lanthanide oxide layers with a combined thickness of the multiple electron beam evaporated lanthanide oxide layers ranging from about 2 nanometers and about 10 nanometers.

66. The electronic system of claim 63, wherein the dielectric layer contains multiple atomic layer deposited hafnium oxide layers with a combined thickness of the multiple atomic layer deposited oxide hafnium oxide layers ranging from about 2 nanometers and about 10 nanometers.

67. The electronic system of claim 63, wherein the atomic layer deposited hafnium oxide layer and the electron beam evaporated lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate having multiple layers of electron beam evaporated lanthanide oxide, each layer of electron beam evaporated lanthanide oxide limited to a thickness of between about 2 nanometers and about 10 nanometers.

68. The electronic system of claim 63, wherein the electron beam evaporated lanthanide oxide layer includes an oxide selected from Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, and Dy_2O_3.